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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,083	10/16/2003	Yasunobu Umemoto	2102487-991121	9080

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,083	UMEMOTO ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1A, 1B and 1C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 12-14 are objected to because of the following informalities: It appears by the context of the new claims that claim 12 should depend from new claim 11, rather than from claim 1, that claim 13 should depend from new claim 11, rather than from claim 1 and that claim 14 should depend from new claim 13 rather than from claim 3. Appropriate acknowledgement and/or correction is required. For the remainder of this action, these dependencies will be used.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Colwell et al.. Colwell et al., Figures 2a and 3, discloses a semiconductor integrated circuit including a plurality of standard cells (100),

four of which are shown in Figure 3, which are arranged adjacent to each other in a cell row and composed of a plurality of MOS transistors (col. 4, line 54),

each standard cell of said cell row being provided with at least one first contact region (130) through which at least one of said MOS transistors is electrically connected to a power potential, at least one second contact region (131) through which at least one of said MOS transistors is electrically connected to a ground potential and first and second substrate regions (108a) and (108b) located in upper and lower sides of the standard cell,

wherein said first substrate region of said each standard cell is joined to the first substrate region of an adjacent cell of said cell row located adjacent to said each standard cell within said each cell row, as shown in Figure 3, for example, in order to form a first substrate continuous region extending along said cell row in parallel while the second substrate region of said each standard cell is joined to the second substrate region of said adjacent cell in order to form a second substrate continuous region extending along said cell row in parallel,

wherein said first substrate continuous region is provided with a plurality of contact regions, which may be embodied as metal lines which may make contact with contact regions (130) or (131) and with various source/drain diffusion region contacts (col. 6, lines 55-56), through which said first substrate is electrically connected to said power potential while said second substrate continuous region is provided with a plurality of contact regions through which said second substrate is electrically connected to said ground potential (col. 6, lines 54-62), and

wherein said first substrate continuous region is provided with a plurality of expanded regions which are extended inwardly toward said standard cells in the longitudinal direction at the location. The expanded regions may be embodied in Figure 2a as centered on the gap between the inner edge of the first substrate region (108a) and the source/drain diffusion region (120), but also may include the immediate edges of the first substrate region and the source/diffusion region. Colwell et al., Figure 2a, discloses that the expanded regions, which may be embodied as being centered on the gap between the inner edge of the first substrate region (108a) and the source/drain diffusion region (120), are formed in spaces which said standard cell can afford.

Claims 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Colwell et al.. Colwell et al., Figures 2a and 3, discloses a semiconductor integrated circuit including a plurality of standard cells (100), four of which are shown in Figure 3, which are arranged adjacent to each other in a cell row and composed of a plurality of MOS transistors (col. 4, line 54),

each standard cell of said cell row being provided with at least one first contact region (130) through which at least one of said MOS transistors is electrically connected to a power potential, at least one second contact region (131) through which at least one of said MOS transistors is electrically connected to a ground potential and first and second substrate regions (108a) and (108b) located in upper and lower sides of the standard cell,

wherein said first substrate region of said each standard cell is joined to the first substrate region of an adjacent cell of said cell row located adjacent to said each standard cell within said each cell row, as shown in Figure 3, for example, in order to form a first substrate continuous region extending along said cell row in parallel while the second substrate region of said each standard cell is joined to the second substrate region of said adjacent cell in order to form a second substrate continuous region extending along said cell row in parallel,

wherein said first substrate continuous region is provided with a plurality of contact regions, which may be embodied as metal lines which may make contact with contact regions (130) or (131) and with various source/drain diffusion region contacts (col. 6, lines 55-56), through which said first substrate is electrically connected to said power potential while said second substrate continuous region is provided with a plurality of contact regions through which said second substrate is electrically connected to said ground potential (col. 6, lines 54-62), and

wherein said first substrate continuous region is provided with a plurality of expanded regions which are extended inwardly toward said standard cells in the longitudinal direction at the location. The expanded regions may be embodied in Figure 2a as centered on the gap between the inner edge of the first substrate region (108a) and the source/drain diffusion region (120), but also may include the immediate edges of the first substrate region and the source/diffusion region.

As to claim 12, the metal lines which may make contact with contact regions (130) or (131) and with various source/drain diffusion region contacts (col. 6, lines 55-56) may be formed within the expanded regions.

As to claim 13, Colwell et al., Figure 2a, discloses that the expanded regions, which may be embodied as being centered on the gap between the inner edge of the first substrate region (108a) and the source/drain diffusion region (120), are formed in spaces which said standard cell can afford.

As to claim 14, the metal lines which may make contact with contact regions (130) or (131) and with various source/drain diffusion region contacts (col. 6, lines 55-56) may be formed within the expanded regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
June 23, 2004

NATHAN J. FLYNN
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